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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/138,578	08/24/1998	TAKESHI KAMEDA	0033-0599P	4264

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EXAMINER
KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/138,578	KAMEDA ET AL.	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/24/1998 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "said first storage means being reset by an input of said fourth pulse" and "said second storage means storing said fourth pulse" as cited in claims 4, 8, and 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 (and thus claims 2 through 9) are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. For example, claim 1 states " A data transmission line used connected continuously ... " does not make sense.

4. Also, claim 1 initially states " ... a data holding unit receiving and holding data transmitted from a preceding stage or data output from an external synchronous system ... " and later states " ... an adjustment unit for adjusting, when a mode in which data output from said synchronous system ... ". So initially, "synchronous system" is within an "or" condition and later "synchronous system" is made into a limitation.

5. Also in claim 1 the following phrase does not make sense " ... an adjustment unit for adjusting, when a mode in which data output from said synchronous system is taken and transmitted to said data transmission line, is designated, timing of input of the data output from said synchronous system and the data transmitted in the asynchronous system from said preceding stage to said data holding unit, by said transfer control unit." What is being adjusted is unclear.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 3, and 7 rejected under 35 U.S.C. 102(b) as being anticipated by Marumatsu et al . 5373204.

8. As per claim 1, Marumatsu teaches a data transmission line used connected continuously in a plurality of stages (Marumatsu fig. 1: stages 10, 20, 30) in an asynchronous system (Marumatsu fig. 1: logic circuits do not have a synchronous clock signal from transfer control circuit and thus it is asynchronous), comprising:

a data holding unit (Marumatsu fig. 1: 22) receiving and holding data transmitted from a preceding stage (Marumatsu fig. 1: 10) or data output from an external synchronous system (Marumatsu fig. 1: 10 is synchronous because it is receiving a synchronized clock from transfer control circuit; the transfer control circuit is synchronous since it has the sync signal), and outputting and transmitting the data to a succeeding stage;

a transfer control unit (Marumatsu fig. 1: 24) for controlling input and output of said data at said data holding unit; and

an adjustment unit for adjusting timing of input of the data output from said synchronous system and the data transmitted in the asynchronous system from said preceding stage to said data holding unit (Muramatsu fig. 1: 14).

As per claim 2, the data transmission line according to claim 1, further comprising buffer means (Muramatsu fig. 1: logic circuits 16, 26, 36) controlled by said synchronous system (Muramatsu fig. 1: 16, 26, 36 are fed data through 12, 22, 32 which are synchronous since 14, 24, 34 provide synchronized clock signals), said buffer means provided between said synchronous system and said data holding unit (Muramatsu paragraph 37: "Meanwhile, it is often necessary to control processing so as to gradually proceed data on a stage by stage basis for each data transmission circuit or logic circuit, when transfer timing of each data transmission circuit is to be verified or the content of processing by a logic circuit disposed between data transfer circuits is to be debugged."), receiving and temporarily holding output data of said synchronous system and outputting the data to said data holding unit.

As per claim 3, the data transmission line according to claim 2, wherein said mode designation is canceled in response to completion of data input to said data holding unit (Muramatsu paragraph 29: " Note that transmission acknowledge signal RO in its "H" level indicates acknowledgement of transfer, while in its "L" level prohibition of transfer. Transfer request signal CI in its "L" level indicates that data transfer is being requested from the preceding stage, while in its "H" level indicates that data transfer is not requested from the preceding stage.").

As per claim 7, the data transmission line according to claim 1, wherein said mode designation is canceled in response to completion of input to said data holding unit (Muramatsu paragraph 29: " Note that transmission acknowledge signal RO in its "H" level indicates acknowledgement of transfer, while in its "L" level prohibition of transfer. Transfer request signal CI in its "L" level indicates that data transfer is being requested from the preceding stage, while in its "H" level indicates that data transfer is not requested from the preceding stage.").

Allowable Subject Matter

Claims 4, 5, 6, 8, and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with the underlined portions:

As per claim 4, the data transmission line according to claim 3, wherein said transfer control unit includes, in order to transfer a first pulse applied from said preceding stage (Muramatsu fig. 2: DI) as a second pulse to said succeeding stage (Muramatsu fig. 2: DO), in accordance with an instruction signal instructing transfer acknowledgement or inhibition (Muramatsu fig. 2: CP via CI and RO),

first storage means for storing said first pulse (Muramatsu fig. 1: 16),

a second storage means (Muramatsu fig. 1: 20) reset in response to inhibition state of said instruction signal (Muramatsu fig. 1: C20, R20),

third storage means (Muramatsu fig. 1: 30) reset in response to an input of said first pulse (Muramatsu fig. 1: output of 26 which is the same as the outputs of 22, 16, and 12) and reset in response to an arbitrary applied third pulse input (Muramatsu fig. 1: CP30 via C30 and R30), and logic means for outputting a fourth pulse (Marumatsu fig. 1: C40) in response to a fact that said first storage means is storing said first pulse, said first pulse is not being applied to said first storage means, said second storage means is reset, said instruction signal is in acknowledged state, and said third storage means is reset (Muramatsu paragraph 29: "Transfer request signal CI in its "L" level indicates that data transfer is being requested from the preceding stage, while in its "H" level indicates that data transfer is not requested from the preceding stage."),

said first storage means being reset by an input of said fourth pulse (not in Marumatsu but applicant's figures do not show this either),

said second storage means storing said fourth pulse (not in Marumatsu but applicant's figures do not show this either) and generating said second pulse; and

said adjustment unit generates, in response to a fact that said first storage means stores said first pulse and said first pulse is not being applied to said first storage means (inherent since if the storage means is storing the pulse, it is inherent that the pulse is no longer being applied to the storage means. The pulse was only being applied to the storage means when the pulse was in the process of being stored in the storage means but the pulse was not in the storage means), ***said adjustment unit generates said third pulse with a desired timing between data transfer of said asynchronous system and a clock of said synchronous system (not in Muramatsu; Muramatsu fig. 1: third pulse as defined before is between the data holding circuits; the adjustment unit which is the transfer control circuit does not generate the third pulse in Muramatsu)***.

(allowable since claim 4 is allowable) As per claim 5, the data transmission line according to claim 4, wherein said data holding unit includes an asynchronous holding circuit for holding data transmitted in said asynchronous system, and a synchronous holding circuit for holding data output from said synchronous system.

(allowable since claims 4 and 5 are allowable) As per claim 6, the data transmission line according to claim 5, wherein said asynchronous system includes a data driven type information processing unit, and said synchronous system includes a clock synchronous information processing unit.

As per claim 8, the data transmission line according to claim 7, wherein said transfer control unit includes, in order to transfer a first pulse applied from said preceding stage (Muramatsu fig. 1:

input to 12) as a second pulse to said succeeding stage (Muramatsu fig. 1: output of 12), in accordance with an instruction signal instructing transfer acknowledgement or inhibition,

first storage means for storing said first pulse,

a second storage means (Muramatsu fig. 1: 22) reset in response to inhibition state of said instruction signal (Muramatsu fig. 1: C20, R20),

third storage means (Muramatsu fig. 1: 30) reset in response to an input of said first pulse (Muramatsu fig. 1: output of 26 which is the same as the outputs of 22, 16, and 12) and reset in response to an arbitrary applied third pulse input (Muramatsu fig. 1: CP30 via C30 and R30), and logic means for outputting a fourth pulse (Marumatsu fig. 1: C40) in response to a fact that said first storage means is storing said first pulse, said first pulse is not being applied to said first storage means, said second storage means is reset, said instruction signal is in acknowledged state, and said third storage means is reset (Muramatsu paragraph 29: "Transfer request signal CI in its "L" level indicates that data transfer is being requested from the preceding stage, while in its "H" level indicates that data transfer is not requested from the preceding stage."),

said first storage means being reset by an input of said fourth pulse (not in Marumatsu but applicant's figures do not show this either),

said second storage means storing said fourth pulse (not in Marumatsu but applicant's figures do not show this either) and generating said second pulse; and

said adjustment unit generates, in response to a fact that said first storage means stores said first pulse and said first pulse is not being applied to said first storage means (inherent since if the storage means is storing the pulse, it is inherent that the pulse is no longer being applied to the storage means. The pulse was only being applied to the storage means when the pulse was in the

process of being stored in the storage means but the pulse was not in the storage means), said ***adjustment unit generates, in response to a fact that said first storage means stores said first pulse said third pulse with a desired timing between data transfer of said asynchronous system and a clock of said synchronous system (not in Muramatsu; Muramatsu fig. 1: third pulse as defined before is between the data holding circuits; the adjustment unit which is the transfer control circuit does not generate the third pulse in Muramatsu)***.

As per claim 9, the data transmission line according to claim 1, wherein

said transfer control unit includes, in order to transfer a first pulse applied from said preceding stage as a second pulse to said succeeding stage, in accordance with an instruction signal instructing transfer acknowledgement or inhibition,

first storage means for storing said first pulse,

a second storage means reset in response to inhibition state of said instruction signal,

third storage means reset in response to an input of said first pulse

and reset in response to an arbitrary applied third pulse input (up to here discussed above), and logic means for outputting a fourth pulse in response to a fact that said first storage means is storing said first pulse, said first pulse is not being applied to said first storage means, said second storage means is reset, said instruction signal is in acknowledged state, and said third storage means is reset (Muramatsu paragraph 29: "Transfer request signal CI in its "L" level indicates that data transfer is being requested from the preceding stage, while in its "H" level indicates that data transfer is not requested from the preceding stage."),

said first storage means being reset by an input of said fourth pulse (not in Marumatsu but applicant's figures do not show this either),

said second storage means storing said fourth pulse (not in Marumatsu but applicant's figures do not show this either) and generating said second pulse; and

10. said adjustment unit generates, in response to a fact that said first storage means stores said first pulse and said first pulse is not being applied to said first storage means, ***said adjustment unit generates said third pulse with a desired timing between data transfer of said asynchronous system and a clock of said synchronous system (not in Muramatsu; Muramatsu fig. 1: third pulse as defined before is between the data holding circuits; the adjustment unit which is the transfer control circuit does not generate the third pulse in Muramatsu)***.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

PK
September 4, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

9/6/02